CAD
Computer Aided Design

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Course web page: www.cs.upt.ro/~todinca
in Teaching, CAD,
Or:
https://staff.cs.upt.ro/~todinca/cad/index.html

Structure of the course

- 2 hours lectures, 2 hours lab per week
- Final grade: 50% lab, 50% exam
- It is possible to replace the written exam with an assignment
- Web page:
  https://staff.cs.upt.ro/~todinca/cad/index.html

Assignments

- There will be:
  - A set of mandatory lab works, which will bring a number of points for lab
  - One or two projects/assignments, at your choice:
    - VHDL modeling of a hardware system
    - Modeling a telecommunication system using the OMNeT++ network simulator
  - The code of the project will be uploaded on the Virtual Campus and the project will be presented
- Each student can freely split the points from the assignment(s) between exam and the lab
- **Each assignment can be realized by one or by 2 students**

VHDL assignment

- The VHDL assignment can be:
- very simple, like a FSM (finite state machine) (for a maximum of 8 out of 10 points)
- or more complex, like a multiplication or division algorithm, etc (for 10 points)
- The code must compile and to produce some simulation results

OMNeT++ Assignment

- The OMNeT assignment has a basic part, and a more advanced part, focused on data collection and interpretation.

- For the first part, the students must realize a working simulation model of telecommunication system
  - The list of assignments is on the web page of the CAD course

- Requirements for the first part:
  - The model must be according to the specifications
  - The code must compile
  - The simulation model must run, at least for a short simulation time
  - It is desirable that it can run -as long as required

OMNeT++ Assignment

- Second part:
  - the focus is on data collection and interpretation
  - The model must run a long time in order to collect meaningful data

- Tasks:

  - To write a very short document, where to present the simulation results in a graphical format.

  - And to briefly explain the results.

CAD: Motivation

- We will learn new techniques for modelling and simulation

- We will write computer programs (more precisely, *models*) that deal with:
  - Simulation time, the structure of the model, behavior of each module, concurrency, events…

- The goals of the course: to perform computer aided design of:
  1. Hardware systems
  2. Telecommunication systems

First goal: designing hardware systems

- Lectures: teaching the VHDL language:
  - Simulation mechanism
  - Behavioral modelling
  - Structural modelling was re-introduced this year, in order to help you at the VHDL assignment
- Labs:
  - VHDL modelling and simulation of
    - a small finite state machine
    - The students can choose a more complex VHDL project: a uP, a peripheral circuit like 8253, 8351, etc, or a fuzzy logic controller (FLC),…
  - For more details see the webpage

Telecom systems

- Lectures:
  - Quality of Service (QoS) and QoS differentiation in Internet
    - Architectures for QoS in Internet: Integrated services (IntServ), **Differentiated services (DiffServ)**
    - Techniques: *scheduling*, *admission control*, *routing*, *congestion control*, *queue management,* etc.
  - Mobile communications:
    - basics, LTE (4G), 5G
- Labs:
  - Learning the OMNeT++ network simulator
  - OMNeT++ model of a part of a telecom system
  - Collection and interpretation of the simulation results

Why VHDL ?

- VHDL is a representative hardware description language (HDL)
- It is a standard language (IEEE 1076-1987)
- It contains features specific to HDLs:
  - Simulation mechanism, simulation time, processes, structural descriptions, configurations, etc.
- It has capabilities specific to high-level programming languages:
  - IF, CASE, LOOP statements, subprograms, etc.

Why OMNeT++ ?

- There are many network simulators:
  - Commercial: OPNET, SES/Workbench
  - Non-commercial: ns2, ns3, …
- OMNeT++ is a free (non-commercial) open-source network simulator
- It is easy to learn and to use:
  - It is based on C/C++ for behavioral modeling
  - Uses predefined functions that model modules' behavior (handleMessage, activity, finish, initialize)

Why OMNeT++ ? (cont'd)

- Can be easily used for high-level modelling
- Has also frameworks for more detailed modelling of IP systems, mobile ad-hoc networks, etc
- Good graphical interface
- Capabilities for displaying and processing simulation results, etc.
- Examples, tutorial, user manual…

References

- [EKP98] Petru Eles, Krzysztof Kuchcinski, Zebo Peng, "System Synthesis with VHDL", Kluwer Academic Publishers, 1998 (chapter 2, mostly for behavioural modelling)
- [Bha95] J. Bhasker, "A VHDL Primer", Prentice Hall, 1995
- [Ash] P. Ashenden, "VHDL Cookbook", www… -mostly for assignments
- [Omn10] OMNeT++ User Manual, Version 4.1. Andras Varga and OpenSim Ltd, 2010. [Online]. Available: http://www.omnetpp.org/
- [Sta07] William Stallings, Data and Computer Communications, Eight Edition, Pearson Prentice Hall, 2007 (for DiffServ)
- Power Point slides

Sources

- The VHDL part of the lectures is based on [EKP98] (for behavioral modelling and dataflow modeling, except BLOCKs, and [Bha95] for BLOCKS, structural modelling, advanced topics) in the sense that the CAD lectures contain ideas, figures and text from [EKP98] and [Bha95] respectively. When other sources are used, it will be mentioned.

- The Omnet part is based mainly on [Omn10], meaning that it contains ideas, text and images from [Omn10], when not stated otherwise.