One Hot encoding for FSMs

Proposed problems

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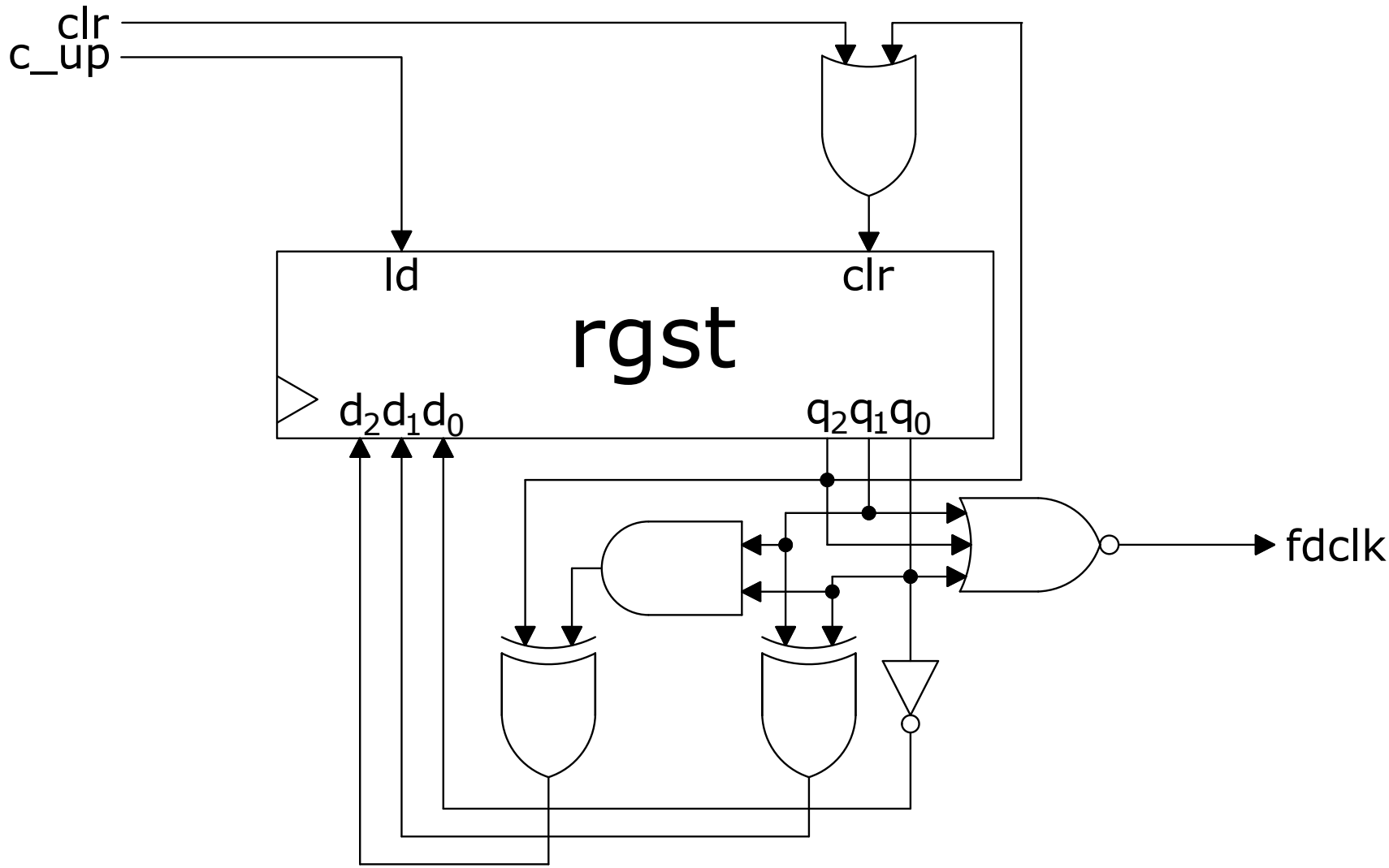
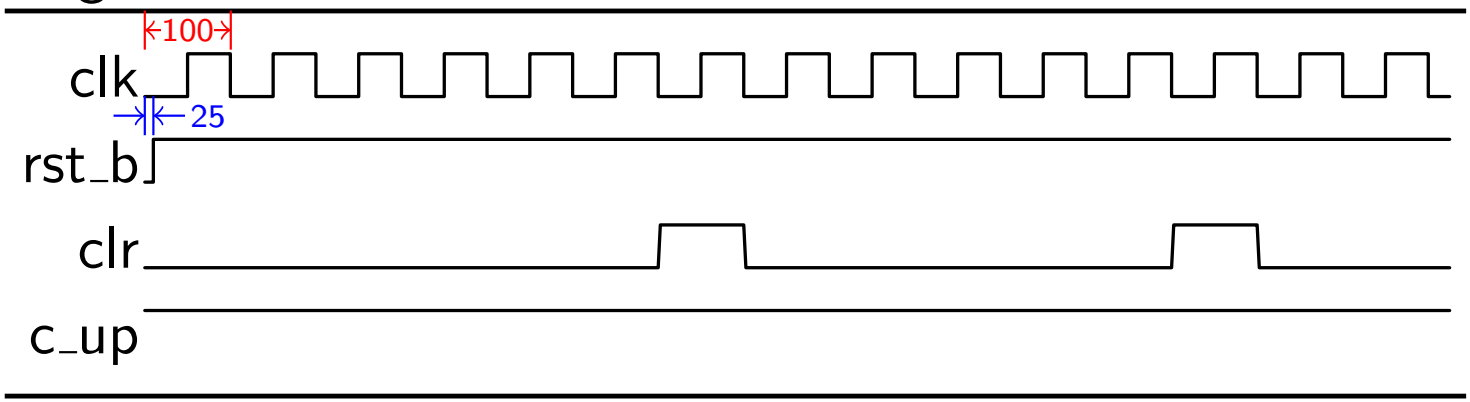
Problem 1

Construct the frequency divider *fdivby5* depicted bellow:



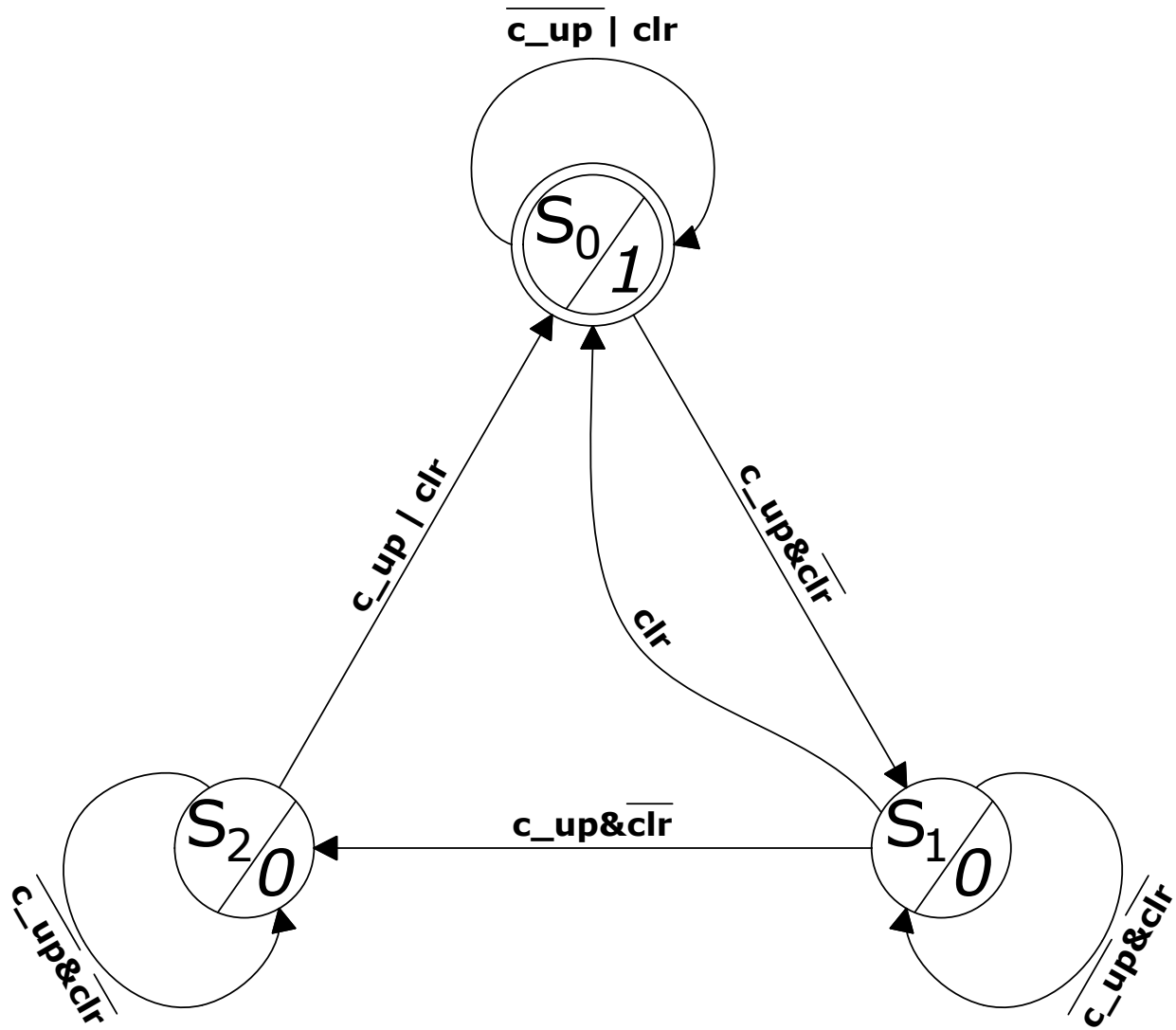
Problem 1 (contd.)

Test the unit with a testbench that generates the inputs as in the diagram bellow:



Problem 2

Prepare the implementation of a One Hot encoded, divide-by-3 frequency divider, called *fdivby3*, whose transition diagram is depicted bellow:

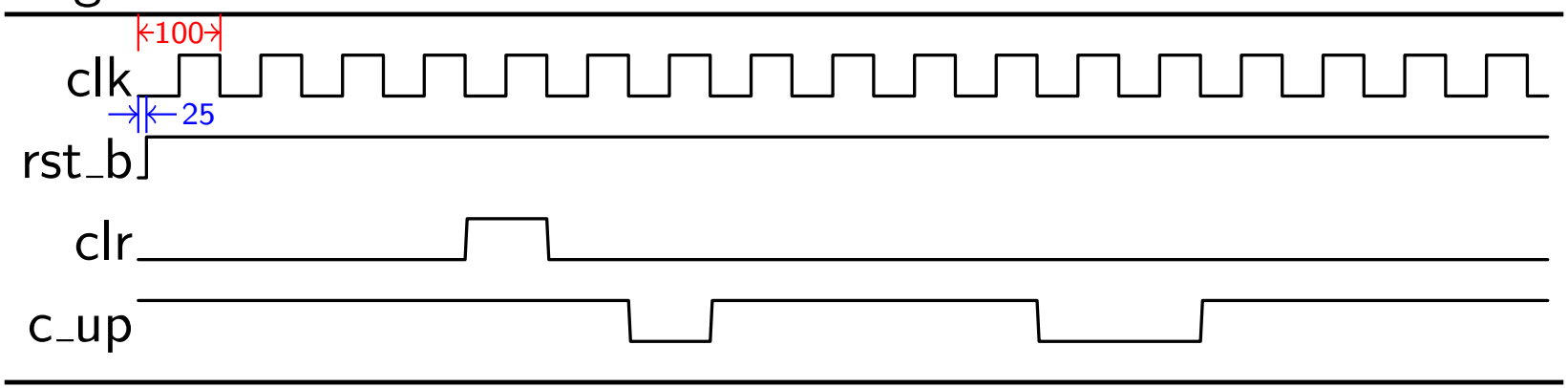


Problem 2 (contd.)

The module will have the following interface:

```
1  module fdivby3 (
2    input clk,rst_b,clr,c_up,
3    output fdclk
4  );
```

Test the unit with a testbench that generates the inputs as in the diagram bellow:



Problem 3

Using the One Hot encoding, implement a divide-by-6 frequency divider that activates its output for 4 consecutive clock cycles (whichever 4 consecutive states).

Test the unit with a testbench that generates the inputs as in the diagram bellow: