Implementing finite state machines in Verilog

Proposed problems

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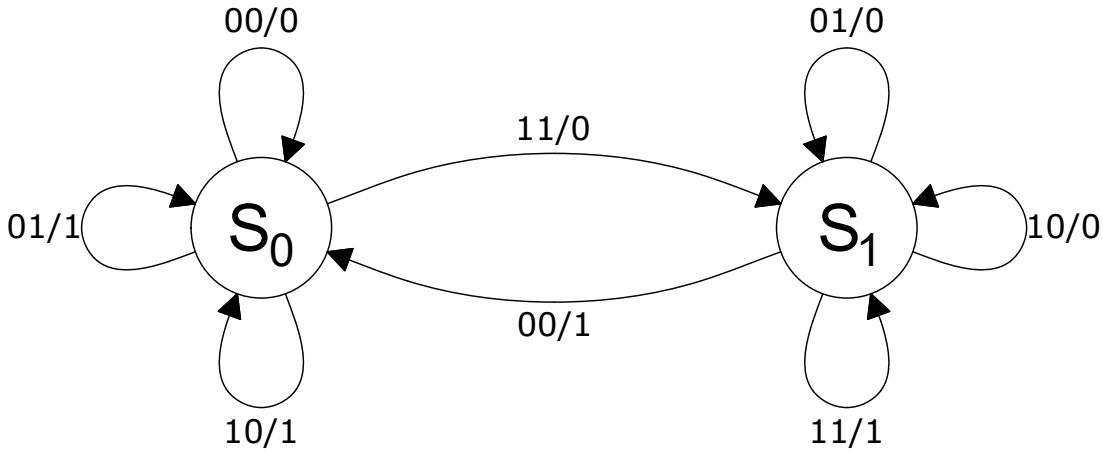
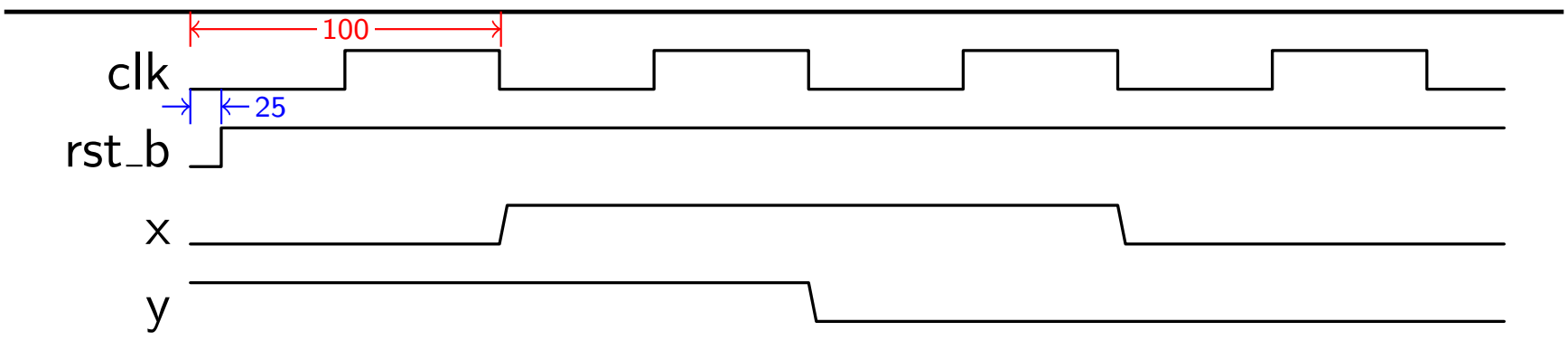
Problem 1

Build the serial adder module, *sadd*, described by the following transition diagram:



Construct a testbench for addition of the 4-bit operands $X = 0110_2$ and $Y = 0011_2$, by generating the inputs as in the timing diagram bellow:



Problem 2

Build a pattern detector module, *patt*, having the 1-bit input *i* and the 1-bit output *o*, capable of detecting at its input the binary sequence 1011. The sequence can be received in an overlapped manner (e.g. for the input sequence 1011011, the output should be activated twice, even though only 7 bits were received).

Build the transition diagram for the machine and implement it.

Construct a testbench and generate module's inputs as in the timing diagram bellow: