Verilog introduction

Proposed problems

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October 2, 2024

Problem 1

Implement the following Boolean functions using only NAND gates in Verilog.

a. $f_1 = \sum(0, 2, 3, 4, 5, 7)$
b. $f_2 = \sum(1, 5, 7, 8, 9, 10, 11, 13, 15)$
c. $f_3 = \sum(0, 4, 5, 15) + \sum_d(2, 7, 8, 10, 12, 13)$
d. $f_4 = \sum(1, 4, 5, 13, 14, 15) + \sum_d(7, 8, 9, 12)$
e. $f_5 = \sum(1, 3, 4, 5, 11, 12, 14) + \sum_d(6, 7, 9)$

Note: For implementing f_1, download file ex1a.v and run_ex1a.txt, complete Verilog code in *ex1a.v* from line 5 and run simulation with `do run_ex1a.txt`.
Similarly, for implementation of f_2 use files ex1b.v and run_ex1b.txt.
For f_3 use files ex1c.v and run_ex1c.txt.
For f_4 use files ex1d.v and run_ex1d.txt.
For f_5 use files ex1e.v and run_ex1e.txt.

Problem 2

Design a module having one input i, as an unsigned on 3 bits and one output o, on 1 bit. The output o is generated as bellow. Implement the unit in Verilog.

$$o = \begin{cases} 1 & \text{if } i = 4k - 3,\ k \in \mathbb{N} \\ 0 & \text{otherwise} \end{cases}$$

Note: For implementing the module, download file ▸ *ex2.v* and ▸ *run_ex2.txt*, complete Verilog code in *ex2.v* from line 5 and run simulation with `do run_ex2.txt`.

Problem 3

Implement the Binary Coded Decimal converter given by the truth table below. Implement it in Verilog.

Inputs				Outputs			
i_3	i_2	i_1	i_0	o_3	o_2	o_1	o_0
0	0	0	0	0	0	0	0
0	0	0	1	0	1	1	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	1
0	1	0	0	0	1	0	0
0	1	0	1	1	0	1	1
0	1	1	0	1	0	1	0
0	1	1	1	1	0	0	1
1	0	0	0	1	0	0	0
1	0	0	1	1	1	1	1

Problem 3 (contd.)

Note: For implementing the module, download file ▸ *ex3.v* and ▸ *run_ex3.txt*, complete Verilog code in *ex3.v* from line 5 and run simulation with `do run_ex3.txt`.

Problem 4

Build a Verilog module, receiving on the 6-bit input *i* non-negative integer numbers. Module's output, on 1 bit is called *is6* and will be active if the decimal's figure of the input number's decimal representation is 6 (Example: $i = 32 \rightarrow is6 = 0$; $i = 60 \rightarrow is6 = 1$; $i = 63 \rightarrow is6 = 1$)

Note: For implementing the module, download file *ex4.v* and *run_ex4.txt*, complete Verilog code in *ex4.v* from line 5 and run simulation with `do run_ex4.txt`.