Optional

Logic families: CMOS family

Doru Todinca

Department of Computers
Politehnica University of Timisoara

CMOS logic levels and noise intervals

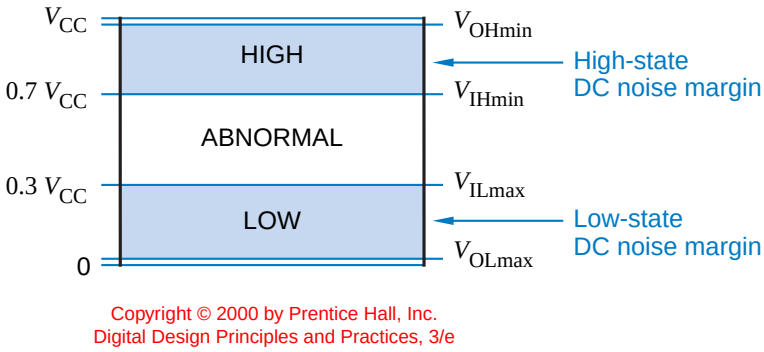


Figure 1 : CMOS logic levels and noise margins

- Figure 1 shows the logic levels for CMOS circuits in function of V_{CC}. Usually $V_{CC} = 5.0V$, but it can be smaller.
- LOW and HIGH mean 0 and 1
- V_{OLmax} is the maximum output voltage that an output in 0 logic can have
- V_{ILmax} is the maximum voltage at an input that is still considered to be a 0 logic
- $V_{ILmax} - V_{OLmax}$ is the noise margin for 0 logic.
- For 1 logic, the output voltage is at least V_{OHmin}, but an input is recognized as 1 if it is $\geq V_{IHmin}$
- Noise margin for 1 logic: $V_{OHmin} - V_{IHmin}$

Model of the MOS transistor

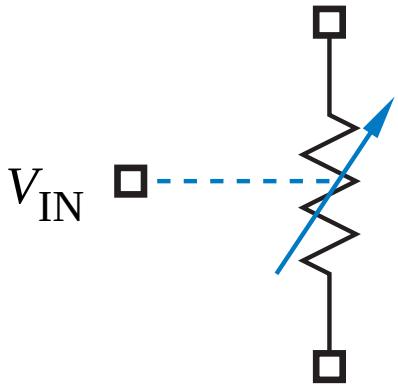


Figure 2 : Model of the MOS transistor as a voltage-controlled resistance

- A MOS transistor is a three terminal device
- An input voltage V_{IN} applied to one terminal controls the resistance between the other two terminals
- In digital circuits the resistance of the MOS transistor is
  - either very high, and the transistor is "OFF"
  - or very low, and the transistor is "ON"

There are two type of MOS transistors: NMOS (with n channel) and PMOS (with p channel).

The n MOS transistor

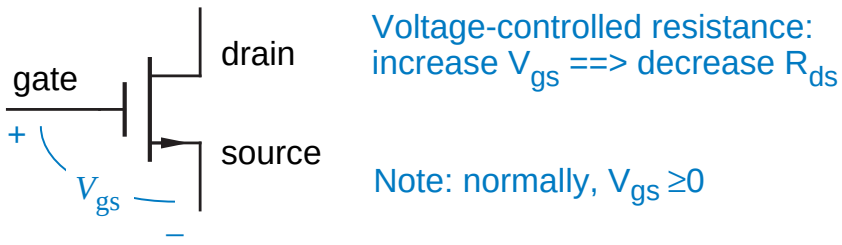


Figure 3 : The N MOS transistor

- The terminals of a MOS transistor are called *gate*, *source* and *drain*
- The drain of an NMOS transistor is normally at a higher voltage than the drain
- The voltage from gate to source, V_{gs} is normally zero or positive.
- If $V_{gs} = 0$ then the resistance from drain to source, R_{ds} is very high (1 megohm or more). The transistor is "OFF"
- When V_{gs} increases, the resistance R_{ds} is very low ($\leq$ 10 ohms) and the voltages in drain and source are almost equal (the transistor is "ON")

The p MOS transistor

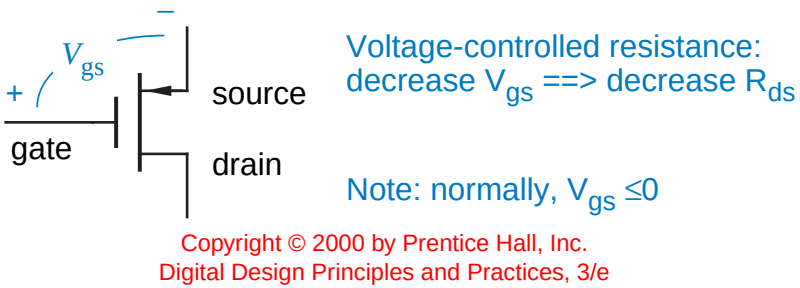
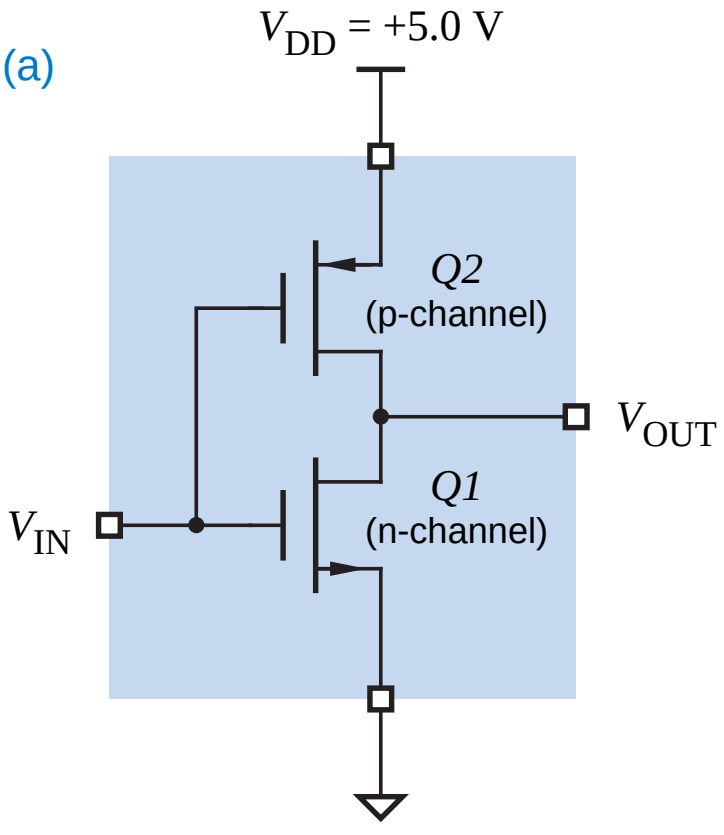


Figure 4 : The p MOS transistor

- The p-channel MOS transistor works similarly, but the source is normally at a higher voltage than the drain
- and normally $V_{gs} \leq 0$
- If $V_{gs} = 0$ the resistance R_{ds} is very high (10^6 ohms), i.e, the transistor is "OFF"
- If V_{gs} decreases algebraically (i.e. $V_{gs} < 0$), then R_{ds} decreases to a very low value and the transistor is "ON": the voltage from drain and source are almost equal.

CMOS NOT gate

(a)



(b)

V_{IN}	Q1	Q2	V_{OUT}
0.0 (L)	off	on	5.0 (H)
5.0 (H)	on	off	0.0 (L)

(c)

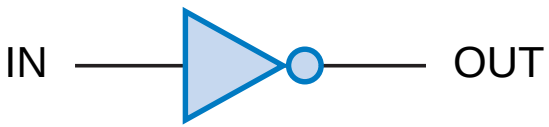


Figure 5 : CMOS NOT gate (inverter): (a) circuit diagram; (b) functional behaviour; (c) logic symbol

CMOS NOT gate

1. If $V_{IN} = 0.0$ V:
   - the NMOS transistor Q1 is OFF because $V_{gs} = 0$
   - the PMOS transistor Q2 is ON because V_{gs} is a large negative value (-5.0 V)
   - It means that Q2 presents only a small resistance between the power supply terminal V_{DD} and the output terminal V_{OUT}
   - It results that $V_{OUT} = 5.0$ V
2. If $V_{IN} = 5.0$ V:
   - Q2 is off because $V_{gs} = 0.0$ V.
   - Q1 is on, since $V_{gs} = 5.0$ V (V_{gs} is large positive)
   - Hence Q1 presents a small resistance between the output terminal and the ground
   - Then, the output voltage is 0 V.

CMOS NOT gate

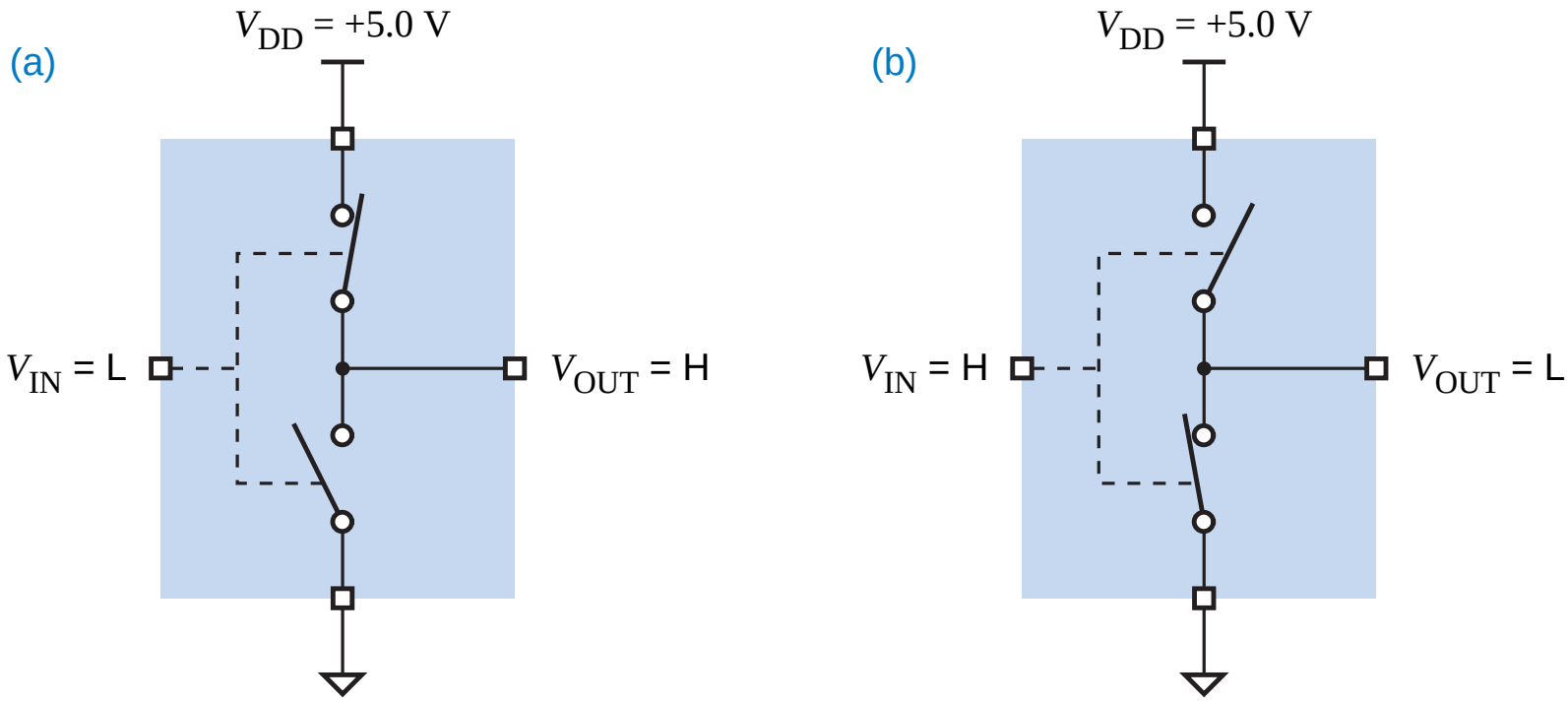


Figure 6 : Switch model for CMOS NOT gate: (a) LOW input; (b) HIGH input

CMOS NOT gate: switch model

- Figure 6 uses switches for modeling the behaviour of an CMOS inverter
- In the left part of the figure (a) the n-channel transistor (bottom) is modeled by a normally-open switch
- The p-channel transistor (top) is modeled by a normally-closed switch
- If we apply a HIGH voltage to V_{IN} the switches go to the opposite position (as shown in (b))
- Based on the switch model we use new symbols for the NMOS and PMOS transistors (in figure 7): PMOS has an inversion bubble at the gate terminal, suggesting that it is ON when V_{IN} is LOW (when V_{IN} is negative).

CMOS NOT gate

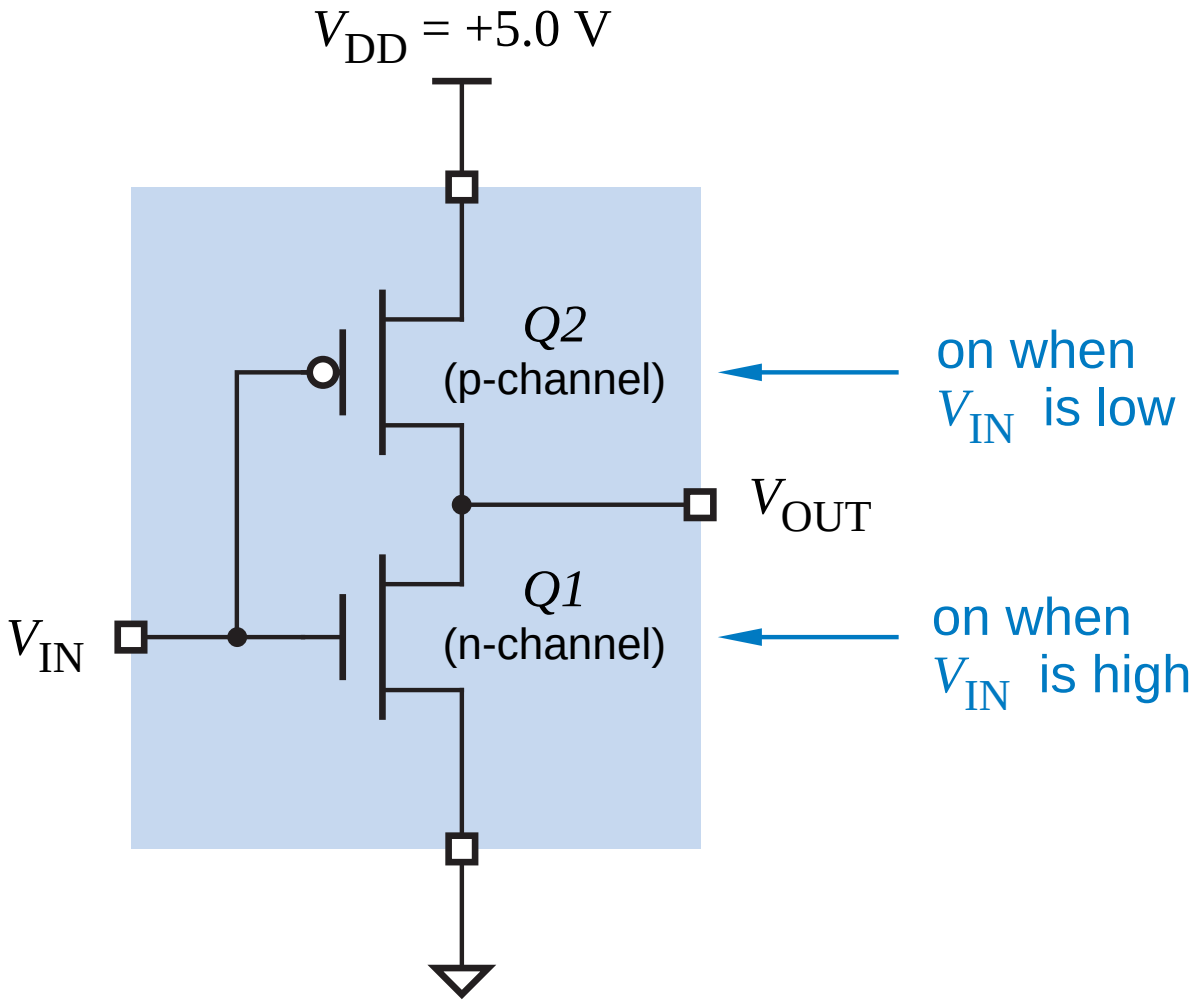
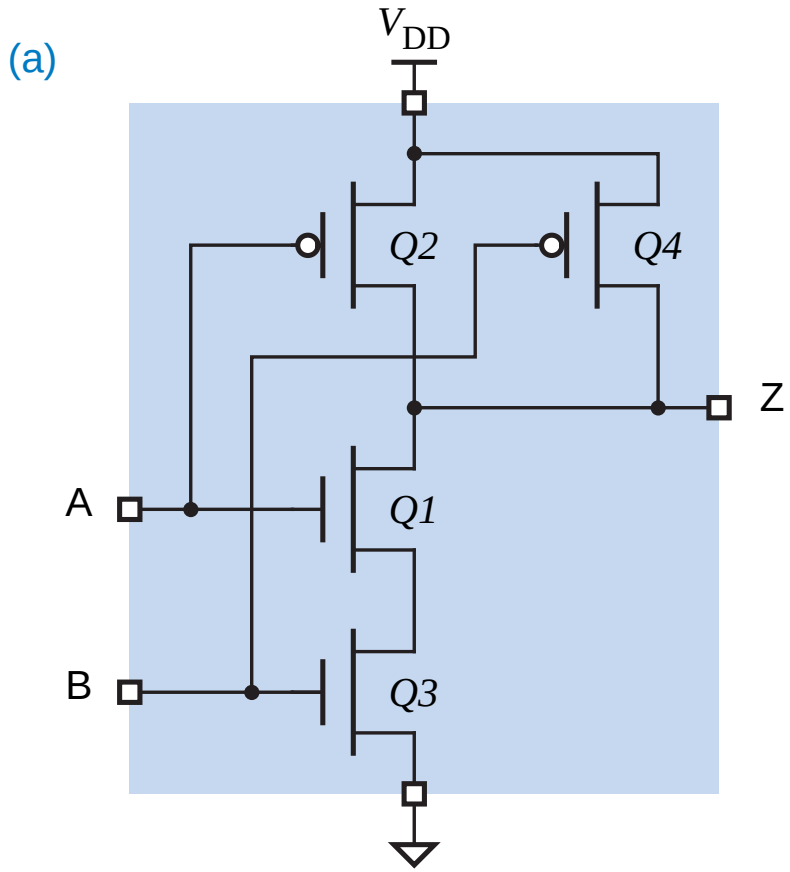


Figure 7 : CMOS NOT gate, different CMOS transistors symbols

CMOS NAND



(b)

A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

(c)

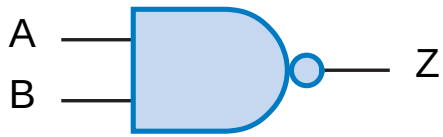


Figure 8 : CMOS 2-inputs NAND gate: (a) circuit diagram; (b) function table; (c) symbol

CMOS NAND

- Circuit diagram of CMOS NAND gate is shown in figure 8
- When at least one input is LOW (0.0 V):
  - the corresponding PMOS transistor(s) will be ON and a path is open between V_{DD} to output Z
  - It results that Z is HIGH
  - The path between Z and ground is blocked because at least one NMOS transistor is OFF
- When both inputs are HIGH (5.0 V):
  - both PMOS transistors are OFF
  - then, the path between V_{DD} and Z is blocked
  - but, both NMOS transistors are ON
  - which means that the path between ground and Z is open
  - hence Z is LOW
  - A switch model of the 2-inputs NAND gate is shown next (in fig 9)

CMOS NAND

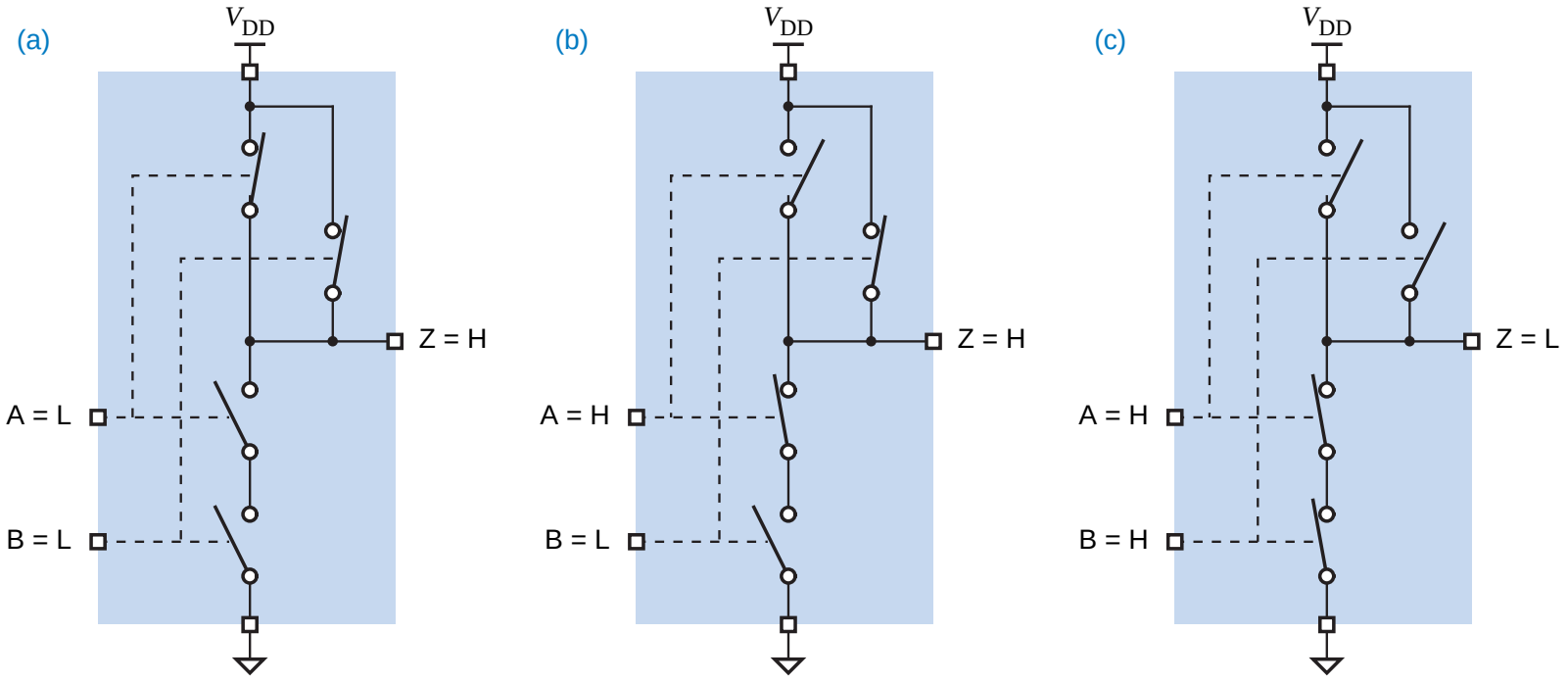
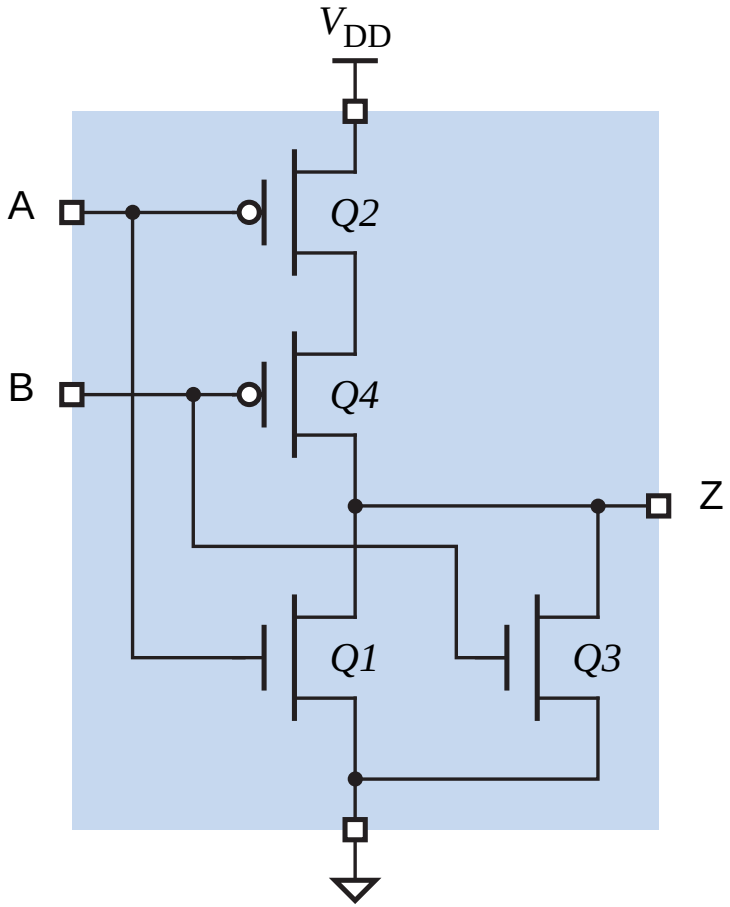


Figure 9 : Switch model for CMOS 2-input NAND gate: (a) both inputs LOW; (b) one input HIGH and one LOW; (c) both inputs HIGH

CMOS NOR

(a)



(b)

A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

(c)

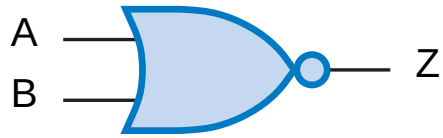


Figure 10 : CMOS 2-inputs NOR gate: (a) circuit diagram; (b) function table; (c) symbol

CMOS NOR

- Figure 10 (a) presents the circuit diagram of CMOS NOR gate
- There is a path between V_{DD} and Z only when both PMOS transistors are ON
- This happens only if all inputs are LOW
- If at least one input is HIGH then the corresponding NMOS transistor(s) is ON
- Which means that there is a path between ground and output Z, hence Z is LOW

CMOS gates

- The family is called CMOS (complementary MOS) because we use pairs of complementary transistors: one NMOS and one PMOS
- Of course, there can be gates with more than 2 inputs
- The CMOS gates have a naturally inverting behaviour
- In order to obtain non-inverting gates (i.e. AND and OR gates) an inverting level must be added to a NAND or NOR gate !
- It means that the non-inverting CMOS gates are slower (and more expensive) than inverting gates (NOT, NAND, NOR)

Input-output transfer characteristic of a CMOS inverter

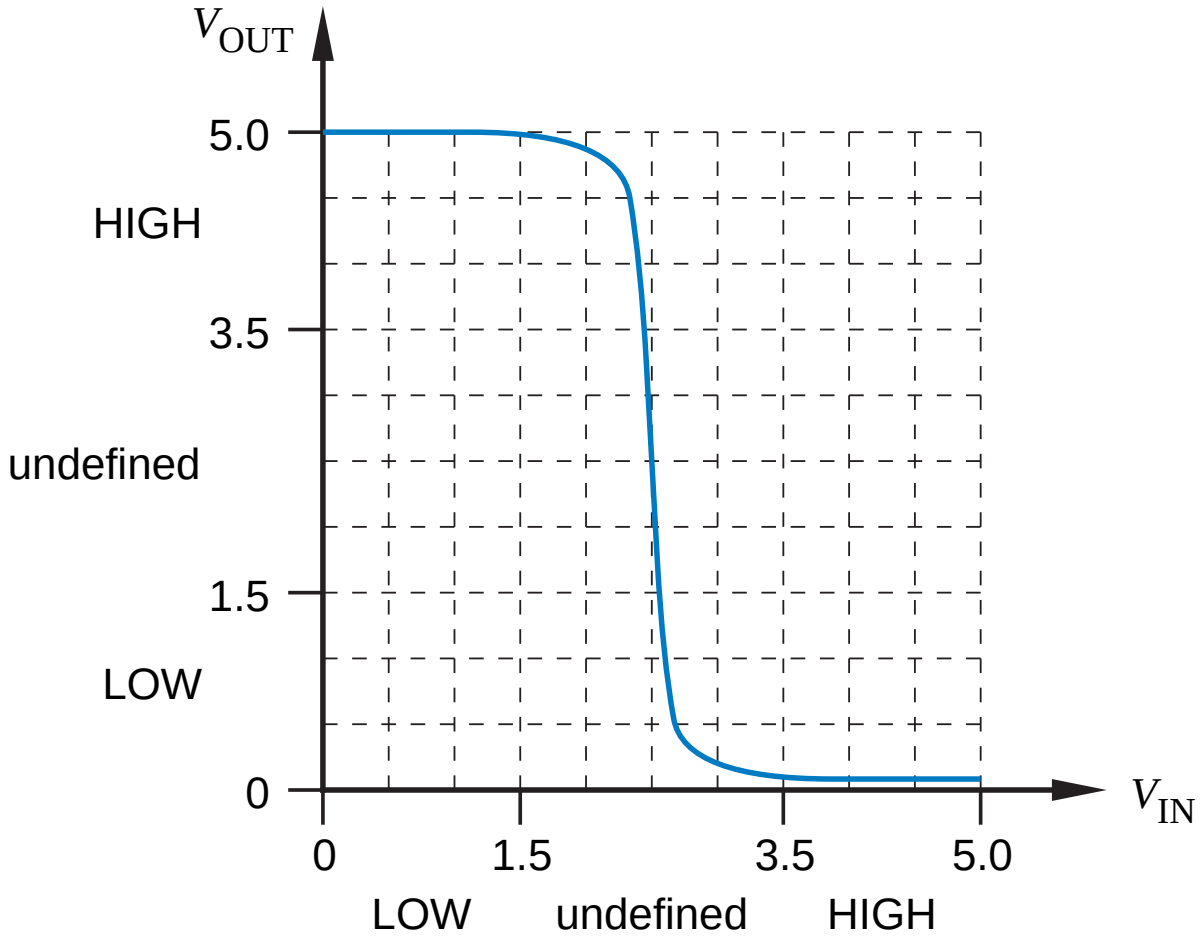


Figure 11 : Input-output transfer characteristic of a CMOS inverter